**Digital Design and Computer Organization Laboratory**

**3rd Semester, Academic Year 2024**

Date: 06/09/2024

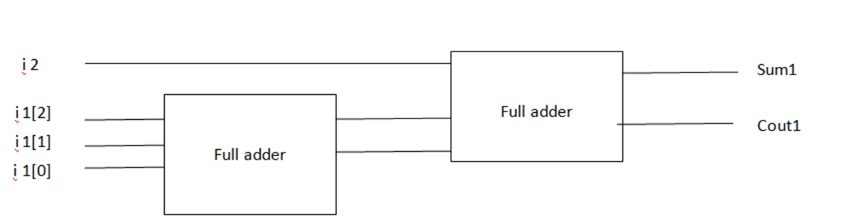
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| --- | --- | --- |
| Name: Rithvik Rajesh Matta | SRN: PES2UG23CS485 | Section: H |

Week#\_\_\_\_5\_\_\_\_\_\_\_

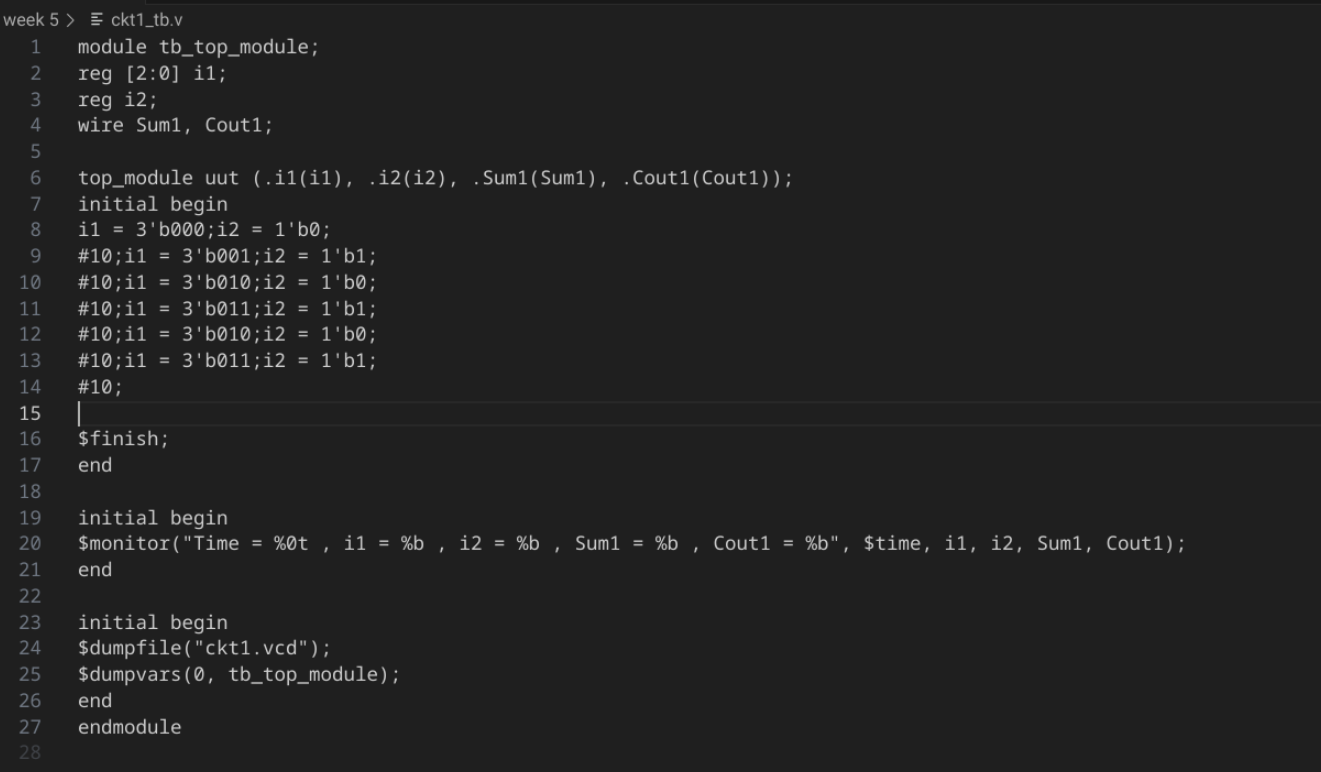
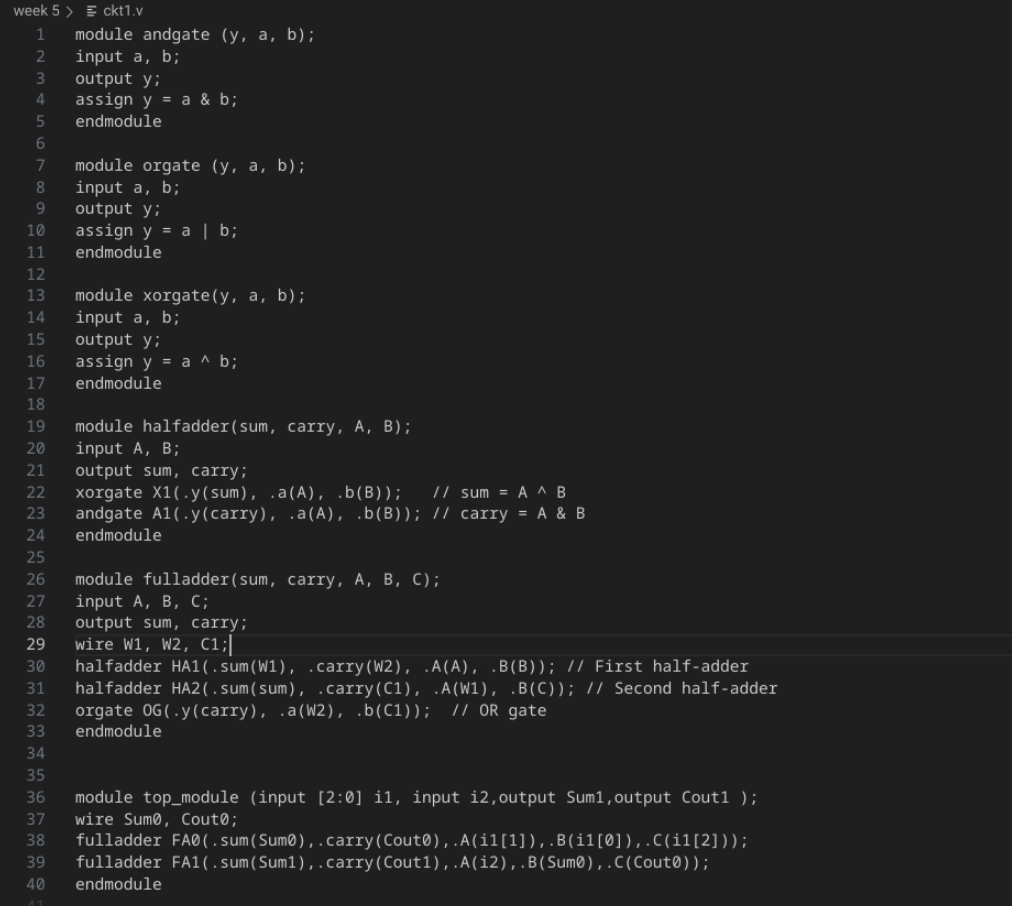
TITLE:

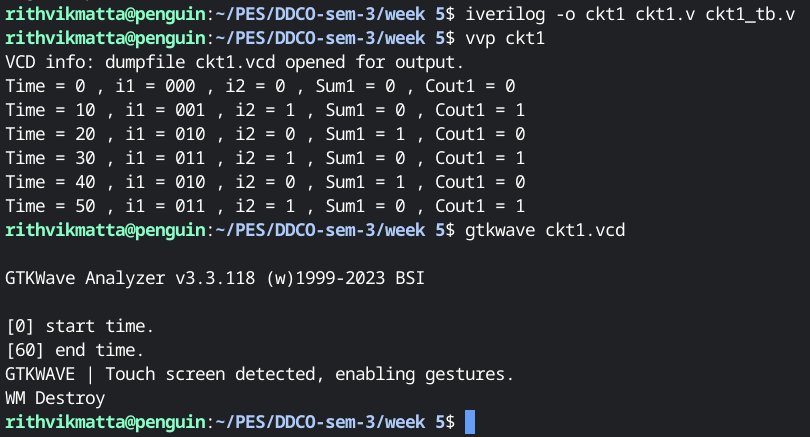
**GENERATE THE VVP OUTPUT AND SIMULATION WAVEFORM USING GTKWAVE. VERIFY THE OUTPUT AND WAVEFORM WITH THE AND GATE TRUTH TABLE**

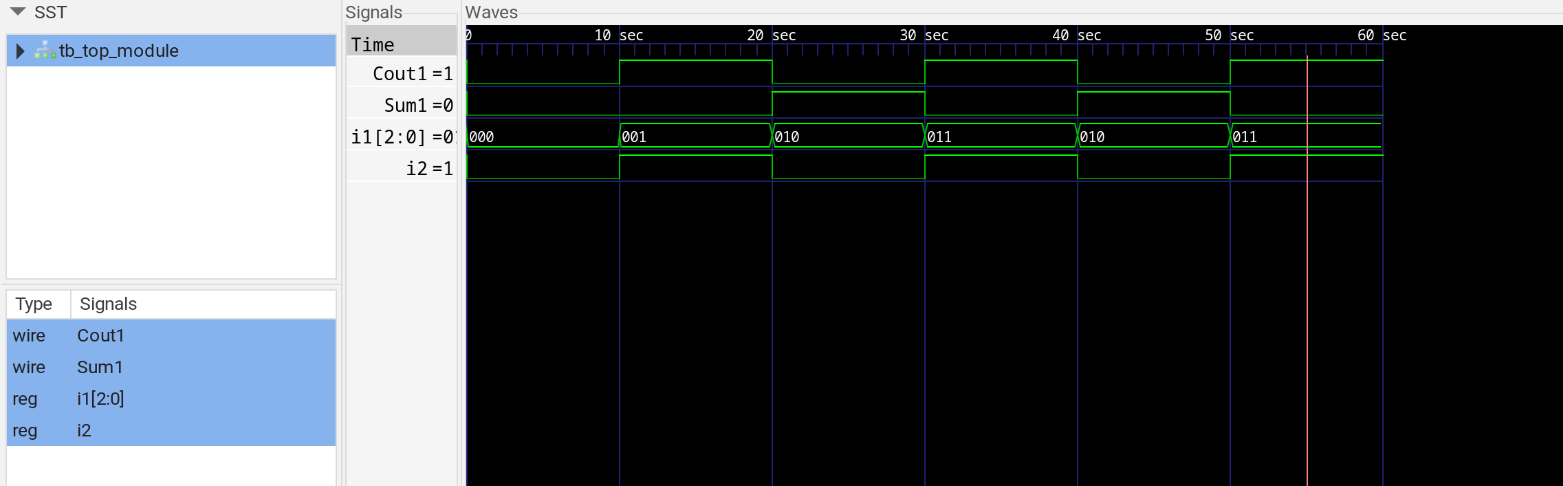
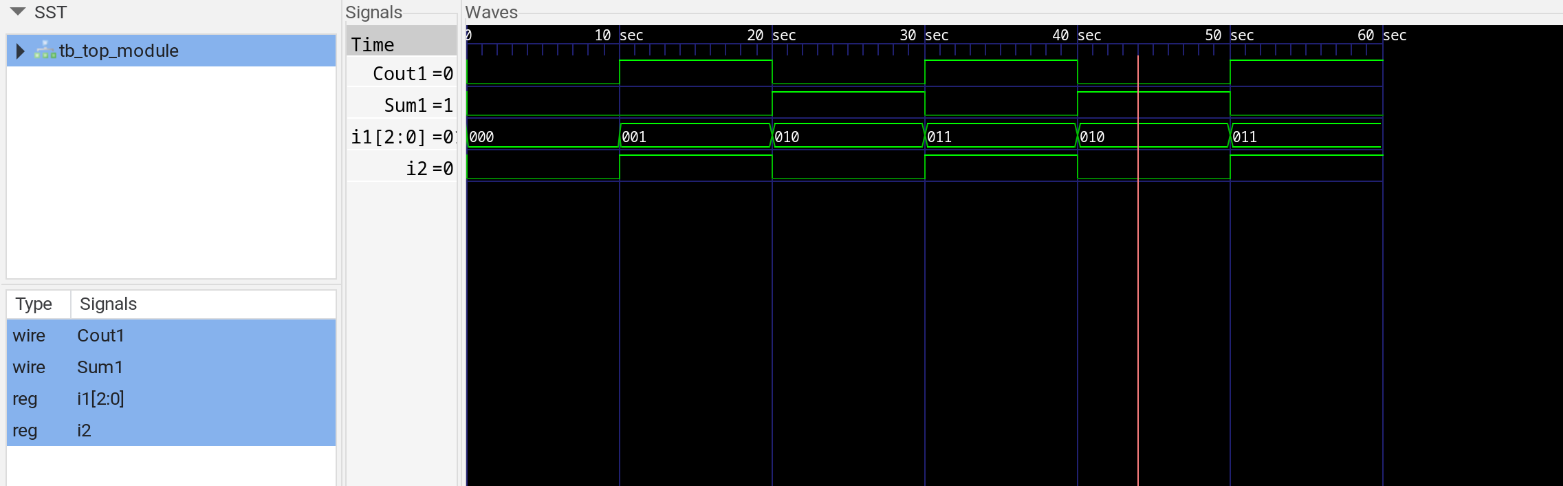
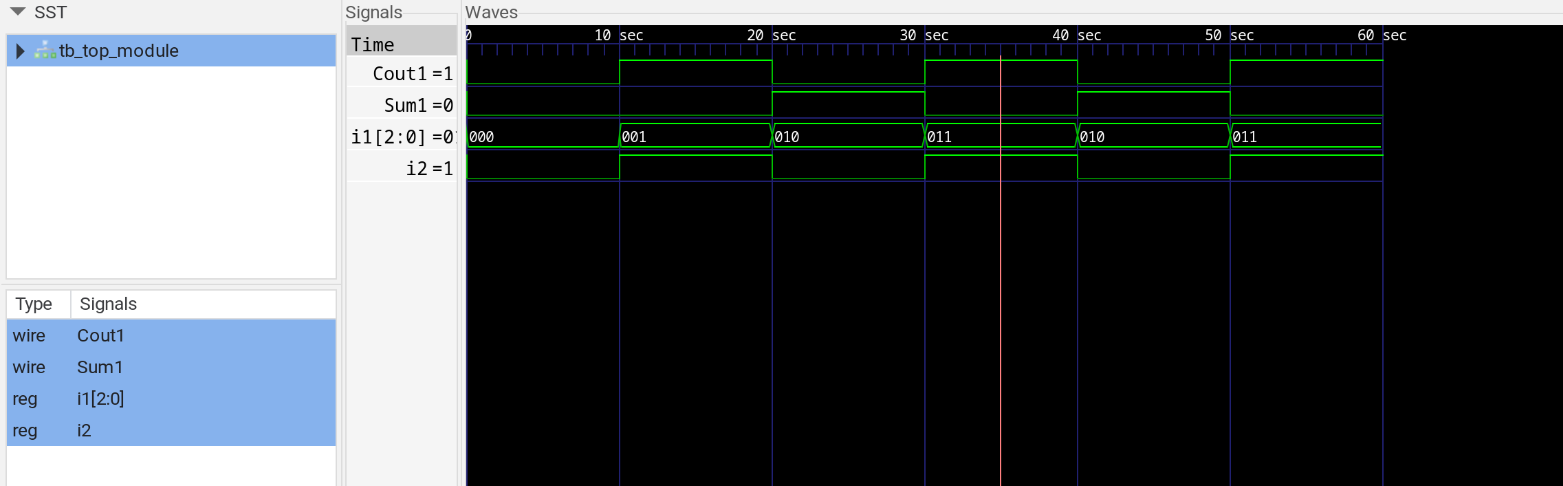
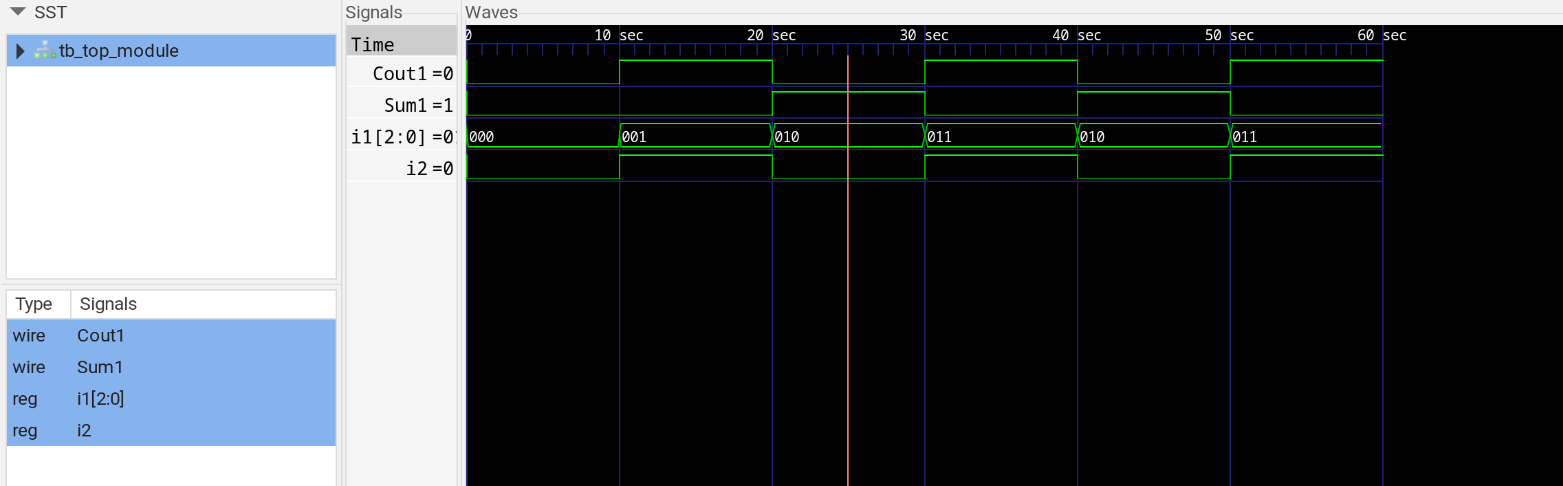
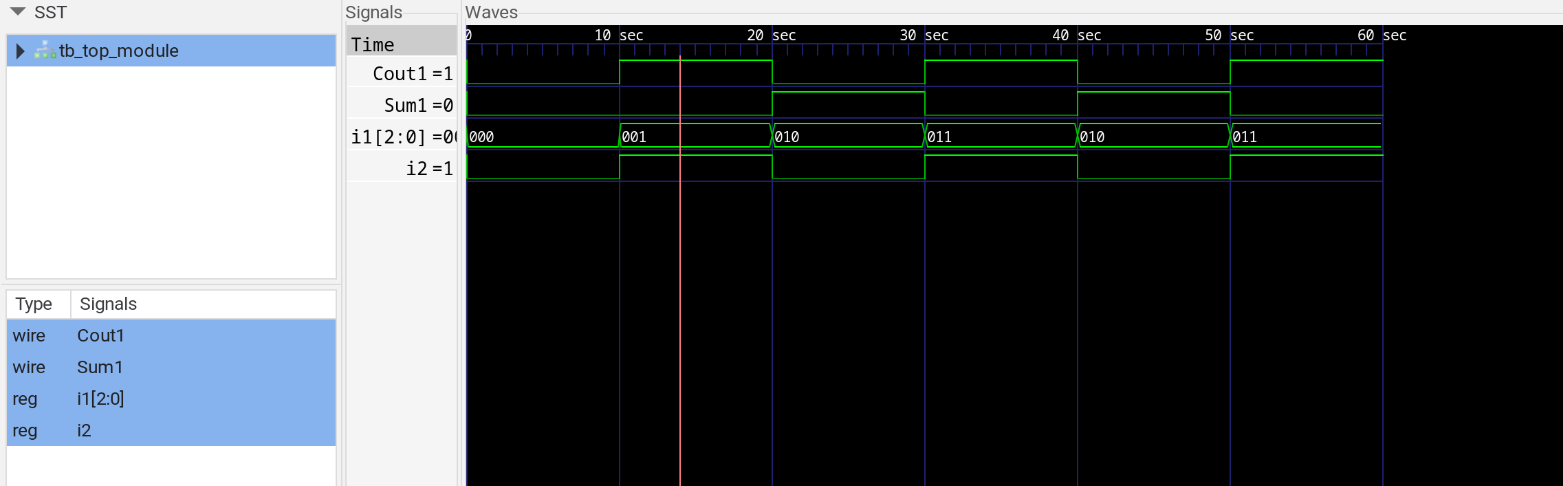
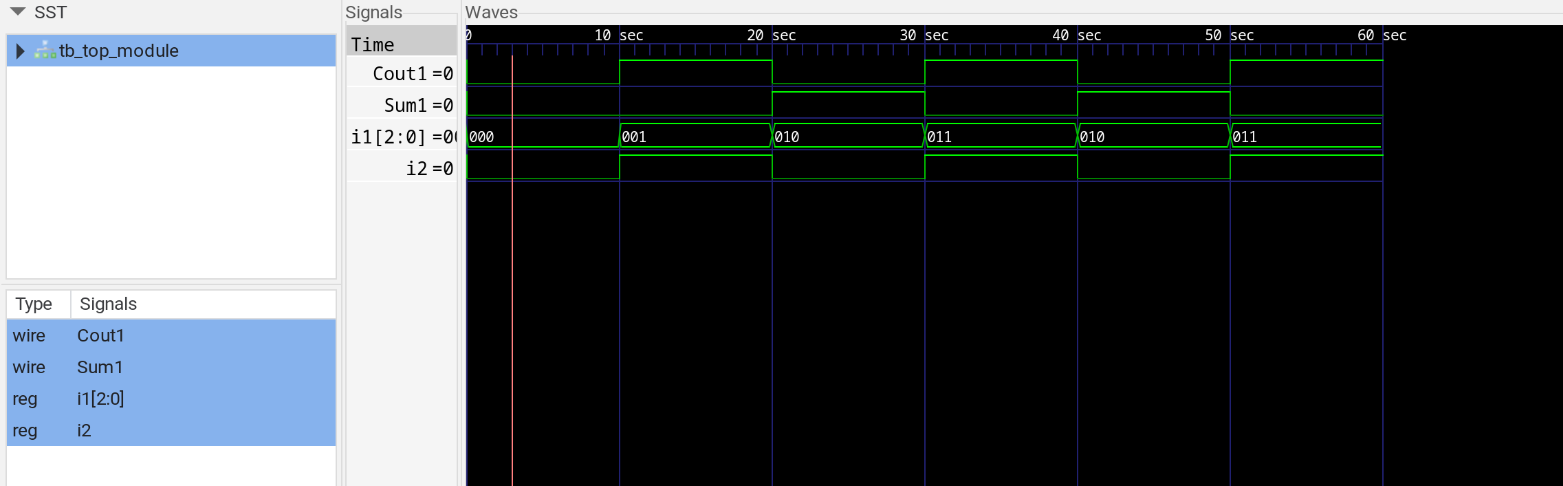
1)Ckt1



|  |  |  |  |
| --- | --- | --- | --- |
| i1 | i2 | Sum1 | Cout1 |
| 000 | 0 | 0 | 0 |
| 001 | 1 | 0 | 1 |
| 010 | 0 | 1 | 0 |
| 011 | 1 | 0 | 1 |
| 010 | 0 | 1 | 0 |
| 011 | 1 | 0 | 1 |







2)ckt2